

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of: Wolfgan GÜNTHER ET AL.
 Appln. No.: Not yet assigned
 Filed: Herewith
 For: METHOD AND DEVICE FOR
 THE EQUIVALENCE
 COMPARISON OF DIGITAL
 CIRCUITS

Examiner: Not yet assigned

Art Unit: N/A

Attorney Docket No: 10808/219

INFORMATION DISCLOSURE STATEMENT

In accordance with the duty of disclosure under 37 C.F.R. §1.56 and §§1.97-1.98, and more particularly in accordance with 37 C.F.R. §1.97(b), Applicants hereby cite the following reference(s):

No.	Date of Publication	Patentee/Applicant/Assignee
5,995,730	November 30, 1999	Blinne
OTHER ART – NON PATENT LITERATURE DOCUMENTS		
Copy of International Examination Report from corresponding PCT patent application No. PCT/EP03/09548.		
R. Drechsler, <i>Equivalence Checking of Digital Circuits in an Industrial Environment</i> , IT+TI Informationstech, Tech. Info., Germany, pgs. 200-205, April 2001.		
Emmanuel Liégeon, <i>Speed Up ASIC Verification Using Formal Verification</i> , Electronique, No. 122, February 2002.		
Subash Chandar G., <i>Addressing Bottlenecks of Fully Synthesized Processor Cores Using Equivalence Checkers</i> , IEEE, pgs. 175-180, 2001.		

Applicants are enclosing Form PTO-1449 (one sheet), along with a copy of each listed reference for which a copy is required under 37 C.F.R. §1.98(a)(2). As each of the listed references is in English, no further commentary is believed to be necessary, 37 C.F.R. §1.98(a)(3). Applicants respectfully request the Examiner's consideration of the above reference(s) and entry thereof into the record of this application.

By submitting this Statement, Applicants are attempting to fully comply with the duty of candor and good faith mandated by 37 C.F.R. §1.56. As such, this Statement is not intended to constitute an admission that any of the enclosed

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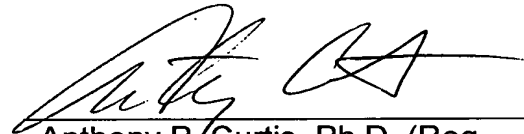
DT01 Rec'd PCT/PTC 25 FEB 2005

references, or other information referred to therein, constitutes "prior art" or is otherwise "material to patentability," as that phrase is defined in 37 C.F.R. §1.56(a).

Applicants have calculated no fee to be due in connection with the filing of this Statement. However, the Director is authorized to charge any fee deficiency associated with the filing of this Statement to a deposit account, as authorized in the Transmittal accompanying this Statement.

Respectfully submitted,

2/25/05
Date



Anthony P. Curtis, Ph.D. (Reg.
No.46,193)

10/526002

FORM PTO-1449	SERIAL NO. Not yet assigned	CASE NO. 10808/219
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE Herewith	GROUP ART UNIT N/A
(use several sheets if necessary)		APPLICANT(S): Wolfgang Günther et al.

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER Number-Kind Code (if known)	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
	A1	5,995,730	November 30, 1999	Blinne		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER Number-Kind Code (if known)	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES OR NO

EXAMINER
INITIAL

OTHER ART – NON PATENT LITERATURE DOCUMENTS

(Include name of author, title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date page(s), volume-issue number(s), publisher, city and/or country where published.

	A2	Copy of International Examination Report from corresponding PCT patent application No. PCT/EP03/09548.
	A3	R. Drechsler, <i>Equivalence Checking of Digital Circuits in an Industrial Environment</i> , IT+TI Informationstech, Tech. Info., Germany, pgs. 200-205, April 2001.
	A4	Emmanuel Liégeon, <i>Speed Up ASIC Verification Using Formal Verification</i> , Electronique, No. 122, February 2002.
	A5	Subash Chandar G., <i>Addressing Bottlenecks of Fully Synthesized Processor Cores Using Equivalence Checkers</i> , IEEE, pgs. 175-180, 2001.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.